

CLAIMS:

- 1 1. A receiver comprising:
2 an input configured to receive serial data;
3 an oscillator configured to generate phases of a clock; and
4 a retiming mechanism configured to receive said serial data and said phases of
5 said clock, wherein said retiming mechanism includes circuitry for reducing timing
6 uncertainties in said serial data by selecting a particular phase of said clock to be
7 asserted to sample said serial data during a period of said serial data.
- 1 2. The receiver as recited in claim 1, wherein each particular phase of said clock
2 to be asserted to sample said serial data during a particular period of said serial data
3 corresponds to a particular retiming state.
- 1 3. The receiver as recited in claim 2, wherein each particular retiming state is
2 paired with a particular synchronization state, wherein said particular synchronization
3 state indicates which particular phase of said clock to assert at a given transition of
4 said serial data signal.
- 1 4. The receiver as recited in claim 3, wherein said retiming mechanism
2 comprises a first unit, wherein said first unit includes circuitry for generating logical
3 values of each particular synchronization state / retiming state pair.
- 1 5. The receiver as recited in claim 4, wherein said first unit receives said phases
2 of said clock and said serial data.
- 1 6. The receiver as recited in claim 5, wherein said first unit comprises a sample
2 clock mechanism configured to sample values of said phases of said clock.

1 7. The receiver as recited in claim 6, wherein said first unit comprises a plurality
2 of second units, wherein said sampled phase values are inputted to said plurality of
3 second units, wherein said plurality of second units includes circuitry for generating
4 said logical values of each particular synchronization state / retiming state pair.

1 8. The receiver as recited in claim 7, wherein said plurality of second units
2 output said logical values of each particular synchronization state / retiming state pair
3 to a completion detector, wherein said completion detector includes circuitry for
4 generating a signal indicating a time to sample inputs of said completion detector.

1 9. The receiver as recited in claim 8, wherein said first unit comprises a third
2 unit configured to detect one of said inputs of said completion detector that has not
3 changed state upon said completion detector generating said signal, wherein said one
4 of said inputs that did not change state corresponds to a particular synchronization
5 state / retiming state pair to be asserted.

1 10. The receiver as recited in claim 7, wherein each of said plurality of second
2 units comprises circuitry for performing a NOR function on particular sampled phase
3 values.

1 11. The receiver as recited in claim 8, wherein said completion detector comprises
2 circuitry for performing a NOR function on said logical values of each particular
3 synchronization state / retiming state pair outputted by said plurality of second units.

1 12. The receiver as recited in claim 1, wherein said oscillator operates at a
2 frequency lower than a data rate of said serial data.

1 13. A system comprising:

2 a transmission medium;

3 a transmitter coupled to said transmission medium, wherein said transmitter is
4 configured to transmit data in a serial form; and

5 a receiver coupled to said transmission medium, wherein said receiver is
6 configured to receive said serial data, wherein said receiver comprises an oscillator
7 configured to generate phases of a clock, wherein said receiver further comprises a
8 retiming mechanism configured to receive said serial data and said phases of said
9 clock, wherein said retiming mechanism includes circuitry for reducing timing
10 uncertainties in said serial data by selecting a particular phase of said clock to be
11 asserted to sample said serial data during a period of said serial data.

1 14. The system as recited in claim 12, wherein each particular phase of said clock
2 to be asserted to sample said serial data during a particular period of said serial data
3 corresponds to a particular retiming state.

1 15. The system as recited in claim 14, wherein each particular retiming state is
2 paired with a particular synchronization state, wherein said particular synchronization
3 state indicates which particular phase of said clock to assert at a given transition of
4 said serial data signal.

1 16. The system as recited in claim 15, wherein said retiming mechanism
2 comprises a first unit, wherein said first unit includes circuitry for generating logical
3 values of each particular synchronization state / retiming state pair.

1 17. The system as recited in claim 16, wherein said first unit receives said phases
2 of said clock and said serial data.

1 18. The system recited in claim 17, wherein said first unit comprises a sample
2 clock mechanism configured to sample values of said phases of said clock.

1 19. The system as recited in claim 18, wherein said first unit comprises a plurality
2 of second units, wherein said sampled phase values are inputted to said plurality of
3 second units, wherein said plurality of second units includes circuitry for generating
4 said logical values of each particular synchronization state / retiming state pair.

1 20. The system as recited in claim 19, wherein said plurality of second units
2 output said logical values of each particular synchronization state / retiming state pair
3 to a completion detector, wherein said completion detector includes circuitry for
4 generating a signal indicating a time to sample inputs of said completion detector.

1 21. The system as recited in claim 20, wherein said first unit comprises a third
2 unit configured to detect one of said inputs of said completion detector that has not
3 changed state upon said completion detector generating said signal, wherein said one
4 of said inputs that did not change state corresponds to a particular synchronization
5 state / retiming state pair to be asserted.

1 22. The system as recited in claim 19, wherein each of said plurality of second
2 units comprises circuitry for performing a NOR function on particular sampled phase
3 values.

1 23. The system as recited in claim 20, wherein said completion detector comprises
2 circuitry for performing a NOR function on said logical values of each particular
3 synchronization state / retiming state pair outputted by said plurality of second units.

1 24. The system as recited in claim 13, wherein said oscillator operates at a
2 frequency lower than a data rate of said serial data.